Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WARREN FARNWORTH
and ALAN WOOD

Appeal No. 2002-1183
Application 08/975,549

ON BRIEF

Before MCQUADE, NASE, and BAHR, Administrative Patent Judges.

MCQUADE, Administrative Patent Judge.

DECISION ON APPEAL

Warren Farnworth et al. appeal from the final rejection of claims 28 through 42, all of the claims pending in the application.

THE INVENTION

The invention relates to "semiconductor manufacture and more particularly to a method . . . for manufacturing known good die" (specification, page 1). According to the appellants, "[k]nown-good-die (KGD) is a collective term that connotes unpackaged die having the same quality and reliability as the equivalent

packaged product" (specification, page 3). Representative claim 28 reads as follows:

28. A method of manufacturing integrated circuits comprising the steps of:
fabricating a plurality of die on a wafer;
segmenting said plurality of die;
performing electrical functionality testing each of said plurality of segmented die to identify satisfactorily nondefective die; and
packaging said satisfactorily nondefective die.

THE REJECTION

Claims 28 through 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,985,988 to Littlebury.

Attention is directed to the appellants' main and reply briefs (Paper Nos. 15 and 19) and to the examiner's final rejection and answer (Paper Nos. 13 and 18) for the respective positions of the appellants and the examiner with regard to the merits of this rejection.

DISCUSSION

I. Preliminary matter

On pages 5 and 7 in the reply brief, the appellants, making the dubious assertion that the examiner has entered a new ground of rejection in the answer, request that we treat the portions of the reply brief relating thereto as a petition under 37 CFR § 1.181(a). We decline to do so because, in addition to being

improperly contained in the reply brief rather than a separate paper (see 37 CFR § 1.4(c)), the request/petition should have been directed to the Commissioner, i.e., the Director, rather than to this Board. We have no jurisdiction to entertain this matter.

II. The merits

Littlebury discloses a method for assembling, testing and packaging integrated circuits. As described by Littlebury with reference to the flow chart depicted in the drawing figure,

> . . . [t]he assembly and test process begins with whole semiconductor wafers which have completed front-end processing. Front-end processing comprises diffusion, photolithography, and metallization processes, while back-end processing refers to packaging, testing, and burning-in the integrated circuits. A first step in the assembly process is burn-in 1 of the integrated circuits. . . .
>
> Preferably, during burn-in 1 the ICs are functionally tested for a first time as indicated by box 2 in the figure. A failure map is produced to record the location of devices which failed during burn-in 1. . . . [A]ny ICs which are not properly burned-in will not be packaged or shipped to a customer. Although the ICs will be tested again later in the assembly process before packaging, only functional test 2, when performed during burn-in, can ensure that burn-in has actually been performed.
>
> A mount and saw process 3 is the next step after the first functional test 2 is done. The wafers are mounted on a supporting film and sawed to separate the individual integrated circuits from each other. . . .
>
> Parametric test 4 is now performed. . . . Parametric testing 4 is different from functional testing 2 in that parametric testing 4 measures important parameters such as operating speed. In

> contrast, functional testing 2 merely tests whether or not the IC is functional, without measuring whether or not the IC meets parameter specifications. . . .
>
> After parametric test 4, a parametric data sort 5 is done so that integrated circuits with similar parameters can be grouped together. . . .
>
> Packaging process 6 and 6' for group one and group two are similar since the integrated circuits themselves are similar except for parameter differences. Integrated circuits from each group are selected from the wafer and placed on leadframes so that each leadframe contains integrated circuits from only one group. . . . After the ICs are bonded to the leadframe, wire bonds are formed coupling contact pads on the integrated circuit to leads on the leadframe. After wire bond, integrated circuits and a portion of the leads are encapsulated, preferably in plastic. . . .
>
> While the packaged integrated circuits are still attached to the leadframe, the packages are marked with an indication of the manufacturer[']s part type and other information, indicated by process steps 7 and 7' in the figure. . . .
>
> After marking 7 and 7', . . . [t]he leads which extend from the package body are trimmed at trim operation 8 so that each of the leads is electrically independent of the others. Trim 8 separates the leads from the leadframe; but tie bars which hold the package to the leadframe are not cut. . . .
>
> Once the leads are electrically isolated from each other, the integrated circuits can be functionally tested once again to identify any failures caused by the assembly process. Second functional test 9 is preferably done in the same piece of equipment as trim 8, sort 10, and sleeve insertion 11 . . . .
>
> Final processing is shown by process blocks 10 and 11 in the figure. After functional test 9 is complete, the leads may be bent into any desired shape to meet a customer[']s specification. After the leads are bent, also called lead forming, the tie bars are cut to remove or singulate the packages from the leadframe.

> The stored functional test data is then used to remove the functional failures which were detected at the previous functional test. Good devices are then transferred into carrier sleeves or boxes which preferably are the same container which is shipped to the customer [column 2, line 34, through column 5, line 29].

As framed by the appellants, the dispositive issue in the appeal is whether Littlebury responds to the limitations in independent claims 28 through 32 requiring functionality testing after die segmentation/singulation and before die packaging. Claim 28, reproduced above, sets forth the steps of "segmenting" a plurality of die from a wafer, "performing electrical functionality testing" of each of the segmented die to identify satisfactorily nondefective die, and "packaging" the satisfactorily nondefective die. Claims 29 through 31 contain comparable limitations, as does claim 32 albeit without a packaging step. The appellants submit that Littlebury "teaches that die are functionally tested on a wafer prior to being singulated and packaged" (main brief, page 5) and "does not provide any teaching or suggestion whatsoever that would lead one skilled in the art to *perform electrical functionality testing after segmentation* of the die" (main brief, pages 5 and 6).

In rejecting the appealed claims as being unpatentable over Littlebury, the examiner takes two approaches to this issue.

First, the examiner concludes that it would have been obvious to one of ordinary skill in the art to substitute an electrical functionality test for Littlebury's parametric test 4 (see page 2 in the final rejection and page 3 in the answer). As so modified, the Littlebury method would meet the claim limitations in question. There is nothing in Littlebury, however, which would have suggested this modification, and the examiner has failed to advance any additional evidence to cure this deficiency. As persuasively argued by the appellants, Littlebury's differentiation between functionality and parametric testing (see column 3, lines 12 through 20) and use of each at intentionally distinct stages of the disclosed method teach away from the proposed substitution, and additionally belie any notion that the artisan would recognize that "functional tests [are] only a sub-species of a parametric test" (answer, pages 5 and 6) as urged by the examiner.

In the alternative, the examiner finds that the electrical functionality testing steps at issue in claims 28 through 32 are met by Littlebury's second functionality test 9, 9' (see page 2 in the final rejection and pages 3 and 7 in the answer). The appellants counter that

> [i]n the Littlebury reference, the second functionality test is performed after the die has been packaged . . . . In contrast, as discussed on page 6 of the Appeal Brief, each of the [independent] claims [28 through 32] recites that the functional testing is performed on "segmented" or "singulated" die, i.e., die that has been cut from the wafer but not yet packaged. Furthermore, some claims, such as claims 28-31, specifically state that the die is packaged subsequent to such testing. Thus, each of the claims recites that the die is functionally [sic, functionality] tested in "segmented' or "singulated" form, while the Littlebury reference teaches that the die is functionally tested in "wafer" form and in "packaged" form. A clearer distinction between claimed subject matter and a cited reference is difficult to imagine [reply brief, page 8].

Notwithstanding the appellants' argument, the examiner's position here is well founded. The specification in the instant application discusses two types of "packaging." The first involves the various lead frame attaching, wire bonding, coating, encapsulating, and finishing procedures depicted as steps 16 through 40 in the prior art process shown in Figure 1, but not in the appellants' inventive process shown in Figure 2, and the second involves the wrapping, boxing, etc., procedures for shipping depicted as step 60 of the prior art process shown in Figure 1 and step 86 of the appellants' inventive process shown in Figure 2. As clearly explained in the specification (see, for example, pages 1 through 8), the appellants' inventive process eliminates packaging of the first type to produce so-called bare

dice. Construed, as they are required to be, in light of the underlying specification, the "packaging" limitations in claims 28 through 31 cover the second type of packaging, but not the first.[1] They therefore read on Littlebury's sleeving or boxing step 11, 11'. Littlebury's second functional test 9, 9' occurs prior to this packaging step and subsequent to the segmentation/singulation step embodied by wafer mounting and sawing step 3. Contrary to the position taken by the appellants, claims 28 through 32 do not require the segmented or singulated die to be devoid of packaging of the first type. Thus, the examiner's determination that Littlebury meets the electrical functionality testing steps respectively set forth in claims 28 through 32 is sound. Indeed, these claims are so broad that it is not evident how the subject matter as a whole recited therein distinguishes over the Littlebury process, or for that matter over the prior art process shown in Figure 1 of the appellants' drawings.

[1] The comments on pages 7 and 8 in the reply brief imply that the packaging limitations in claims 28 through 32 refer to packaging of the first type. If this were the case, however, it would be arguable that the claimed subject matter would lack written descriptive support in the specification as required by 35 U.S.C. § 112, first paragraph, and would not point out and claim the subject matter the appellants regard as their invention as required by 35 U.S.C. § 112, second paragraph.

Thus, the appellants' position on appeal that their invention is patentable over Littlebury is not persuasive. We shall therefore sustain the standing 35 U.S.C. § 103(a) rejection of independent claims 28 through 32, and dependent claims 33 through 42, as being unpatentable over Littlebury.

SUMMARY

The decision of the examiner to reject claims 28 through 42 is affirmed.

AFFIRMED

JOHN P. MCQUADE Administrative Patent Judge	)	
	)	BOARD OF PATENT
	)	APPEALS AND
JEFFREY V. NASE Administrative Patent Judge	)	INTERFERENCES
JENNIFER D. BAHR Administrative Patent Judge	)	

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